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Design of Different Types of Full Adders using Double gate MOSFET Technique

P.A. IRFAN KHAN

Abstract

The full adder circuit is an important cell in many processing systems. The full adder circuit is used to add the partial product of multiplier designs. Decreasing the number of transistor count in full adder can result in less power consumption. In this paper, different types of full adders have been implemented using Double Gate MOSFET technique which is mainly used to reduce the short channel effects in the circuits. These circuits have been implemented using TANNER EDA tool, so this result decreasing the total power consumption and delay of full adder.

Keywords:

Full Adder
CMOS
Double Gate MOSFET
Power Delay Product

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1. Introduction

In many processors multipliers are main building blocks, and these multipliers are constructed using full adders, so full adder circuits plays a vital role in manufacturing the processors. To reduce the power consumption of the processor we need to reduce the power consumption of the full adder. One of major concern for the power consumption is due to short channel effects and these short channel effects can be reduced by Double gate MOSFET technique [1]. Therefore the design of low power VLSI circuits has been increasing due to the demand of portable devices like palmtops, cellular and mobiles. DGMOSFET compared with Single Gate MOSFET has 93% reduction of leakage current, 24% reduction in power consumption and60% reduction in Power Delay Product (PDP) with respect to input voltage [2]. Further to integrate more number of devices on chip, scaling of device size is required. Hence we implement the different types of full adder using Double Gate MOSFET (DGMOSFET).

1.1 Full Adder

Adders are combinations of logic gates that combine binary values to obtain a sum. The full adder becomes necessary when a carry input (Cin) must be added to the two binary digits (A, B) to obtain the correct sum, which add 8, 16, 32, etc. binary numbers [3]. One method of constructing a full adder is to use two half adders and an OR gate as shown in the figure 1.1.

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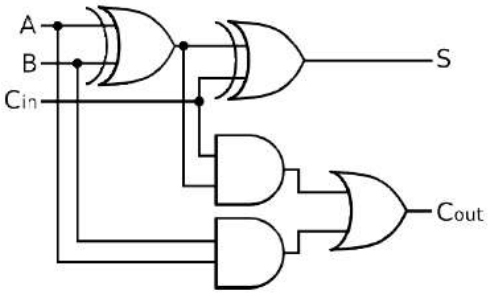

Figure 1.1. Full adder Circuit

The truth table for the full adder circuit is given below.

Table 1.1. Truth table of Full Adder

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

1.2 Double Gate MOSFET (DGMOSFET)

DGMOSFET is one of the promising technologies for transistor design. To accommodate future technology nodes, transistor dimensions have to be reduced which leads to several disadvantages in transistor function. By using double-gate transistors many of these problems can be resolved to give efficient circuit performance. Double-gate transistor allows only one input differential pair to be used. Double Gate MOSFET

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(DG MOSFET) is widely used in ultra-low power design [4]. DGMOSFET's has drain, source and two gates. The two gates (front and back) are electrically coupled together in double gate devices. The structure of double gate MOSFET is shown in figure 1.2.

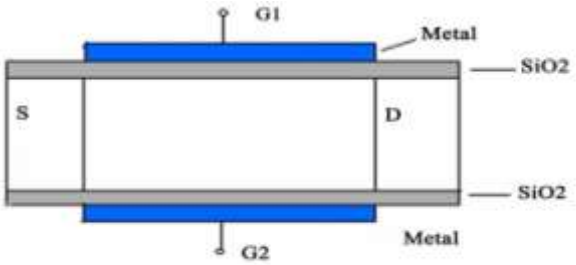

Figure 1.2. Structure of DG MOSFET

2. Research Method

In this paper to reduce the power of the full adder circuit we reduce the total number of transistors of the adder i.e. 28T and 20T.

28T Full adder

To reduce the power consumption of the full adder best method is to reduce the total number of transistors of the adder circuit. To reduce the number of transistor one way is to reduce the equation of sum and carry [5]. Use the carry equation to form a sum which results reduce the number of transistors to 28 from 46 transistors. The circuit diagram of the 28T full adder is shown in below figure 2.1.

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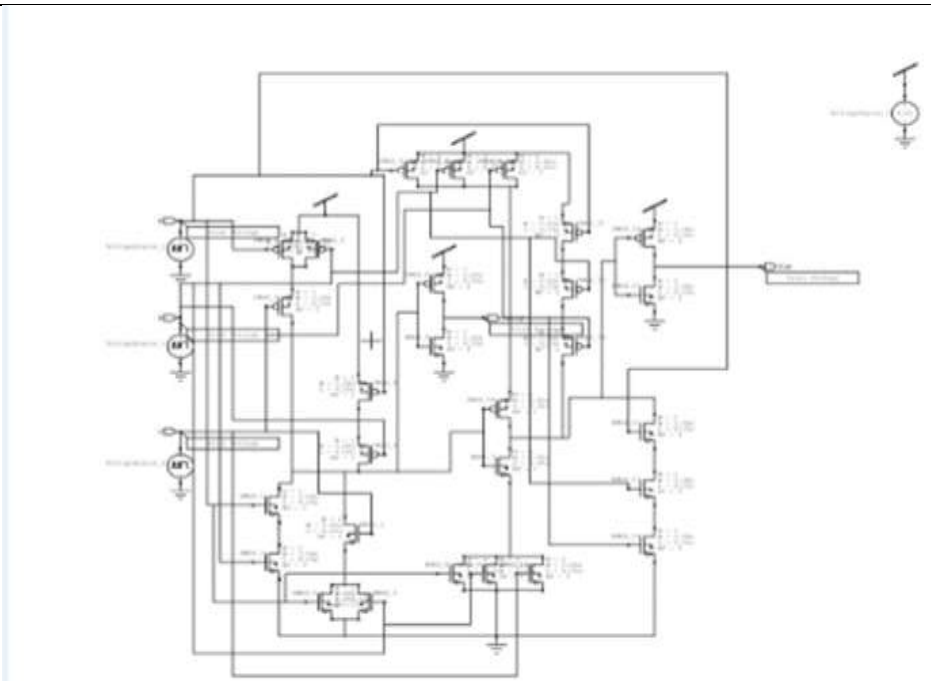

Figure 2.1. 28T Full Adder Circuit

20T full Adder

In this type of full adder we use only 20T to develop a full adder circuit which causes more reduction in power and delay of the full adder circuit. The circuit diagram of this is shown in below figure 2.2.

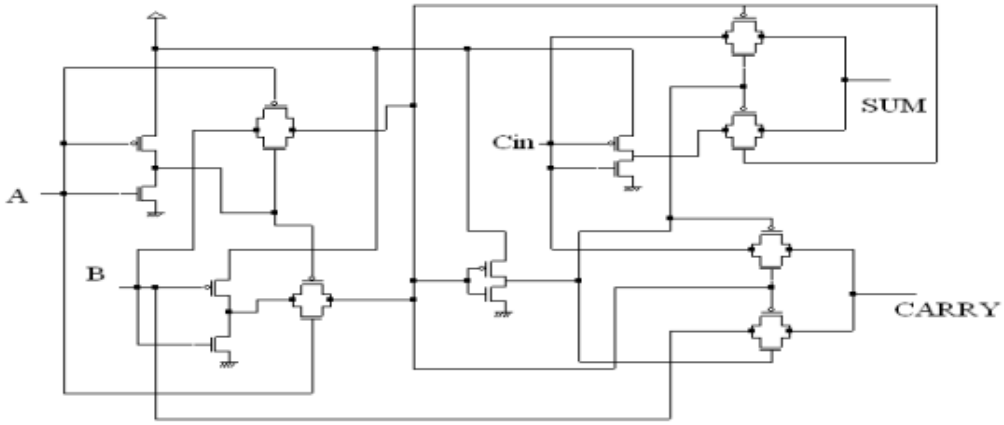

Figure 2.2. 20T Full Adder Circuit

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3. Results and Analysis

In this section we implemented the full adder circuits using double gate MOSFET technique to reduce the power and delay of the full adder circuit. Implementation of 20T full adder circuit is shown in figure 3.1.

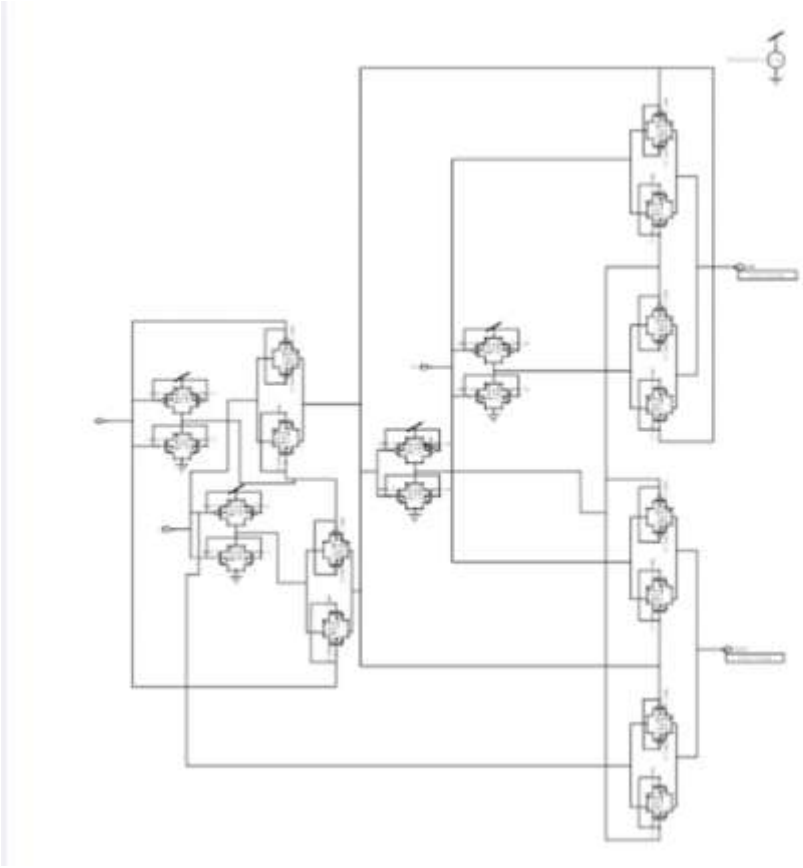

Figure 3.1. 20TFull Adder using DGMOSFET

The output wave of the double gate MOSFET full adder circuit is shown in figure 3.2

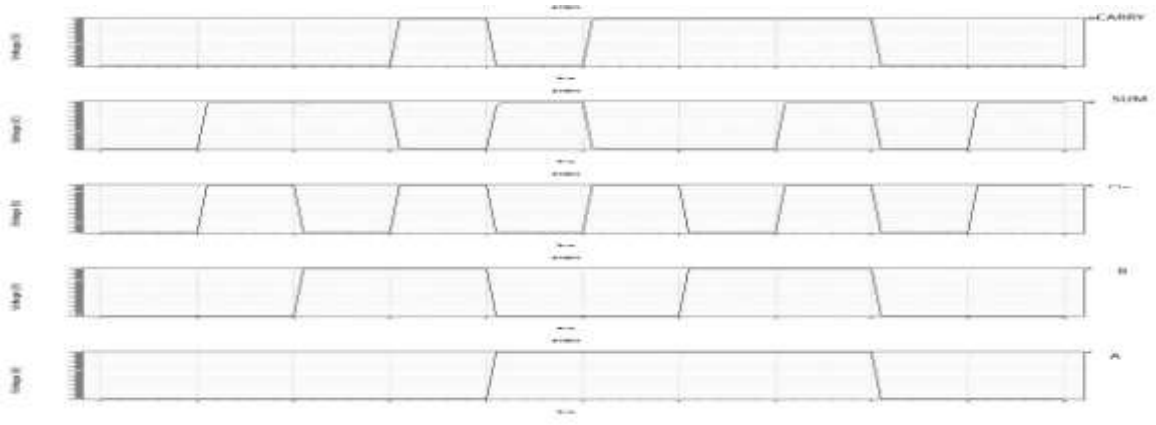

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Figure 3.2. Output Waveform of 20T Full Adder using DGMOSFET

From the above figure 3.2, it can be explained that when A=0,B=0,Cin=0 then the Sum=0 and Carry=0. When A=1,B=1,Cin=1 then the Sum=1 and the Carry=1. If inputs belike A=1,B=1,Cin=0 then the sum=0 and Carry=1. Lets take another sequence be A=0,B=1,Cin=0 then Sum=1 and Carry=0.
The comparison of power and delay of the different full adders is given below.

Table 3.1 Comparison of Power and Delay of Full Adders

BLOCK	**CONVENTIONAL**		**DOUBLE GATE MOSFET**	
	POWER	DELAY	POWER	DELAY
Conventional Full Adder	1.4×10^{-4}	4×10^{-8}	1.6×10^{-2}	7.18×10^{-12}
28T Full Adder	3.76×10^{-6}	3.98×10^{-8}	8.3×10^{-4}	9.77×10^{-9}
20T Full Adder	9.01×10^{-5}	1.99×10^{-9}	1.45×10^{-4}	8.89×10^{-12}

Table 3.2. Comparison of Power Delay Product of Full Adders

BLOCK	**CONVENTIONAL**	**DOUBLE GATE MOSFET**
	POWER DELAY PRODUCT	POWER DELAY PRODUCT
Conventional Full Adder	5.6×10^{-12}	11.48×10^{-14}
28T Full Adder	14.9648×10^{-14}	81.091×10^{-15}
20T Full Adder	17.9299×10^{-14}	12.8905×10^{-16}

In the above table we compare the power delay product of the different full adders because power delay product shows the overall performance the system. From the above table observed that power delay product is much less using double gate MOSFET full adder compared to conventional Full adder.

4. Conclusion

Double Gate MOSFET technology achieves low leakage and high performance operation with high speed. Different parameters are analyzed at various voltage supplies. The power consumption is reduced for DG-MOSFET based full adder cell as compare to other. It is observed that power delay product with

frequency and temperature is better for DG-MOSFET based full adder circuit. The proposed circuit has higher speed and low power while it intact the digital characteristics. The delay of the circuit is reduced by Double gate MOSFET which in turn increases the speed of operation. Moreover DG-MOSFET reduces short channel effect which is a major concern. Simulation results of the full adders have been performed on Tanner EDA v13.0.

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